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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/665,614	09/19/2003	Kazumi Inoh	79001-2037	6405

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EXAMINER	
MANDALA, VICTOR A	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 12/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/665,614	INOH ET AL.	
	Examiner	Art Unit	
	Victor A Mandala Jr.	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 August 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) *13-19 and 26* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12 and 20-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 September 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4-12-04 & 9/19/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Claim13-19 & 26 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected Species, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 8/26/04.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 2, 5, 8, 11, 22, & 25 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 2, 5, 8, 11, 22, & 25 recites the limitation the base. There is insufficient antecedent basis for this limitation in the claim, (See * below).

Claims 2, 5, 8, 11, 22, & 25 recites the limitation the top. There is insufficient antecedent basis for this limitation in the claim, (See * below).

Claims 5, 11 & 25 recites the limitation the bottom. There is insufficient antecedent basis for this limitation in the claim, (See * below).

* The terms top, base, and bottom are used in these claims as regions or elements, which are later compared with the amount of area that they contain, where the rest of the claims that contain these terms use them to justify location and for that reason the rejection is made.

Drawings

3. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the top, base, and bottom regions, (See also * above), must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-6 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,630,714 Sato et al.

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

4. Referring to claim 1, a semiconductor device comprising: a semiconductor substrate, (Figure 17 #60); flat-plate-shaped cavity, (Figure 17 #71), made in the semiconductor substrate, (Figure 17 #60); and an element isolating region, (Figure 17 #73), formed in the surface of the semiconductor substrate, (Figure 17 #60), and located at the sides the cavity, (Figure 17 #71).

5. Referring to claim 2, a semiconductor device, wherein the area of **the top** of the cavity, (Figure 17 #71), is larger than the area of **the base**, (Figure 17 #72), an element region provided at the top the cavity, (Figure 17 #71).

6. Referring to claim 3, a semiconductor device, wherein the element isolating region, (Figure 17 #73), and the cavity, (Figure 17 #71,) enclose the element region, (Figure 17 #72), provided at the top of the cavity, (Figure 17 #71), and electrically separate the element region, (Figure 17 #72), from the semiconductor substrate, (Figure 17 #60).

7. Referring to claim 4, a semiconductor device, wherein only one element region, (Figure 17 #72), provided at the top of the cavity, (Figure 17 #71).

8. Referring to claim 5, a semiconductor device, wherein **the base**, (Figure 17 #72), of the element isolating region is less deep than **the bottom** of the cavity, (Figure 17 #71), and deeper than **the top** of the cavity, (Figure 17 #71).

9. Referring to claim 6, a semiconductor device, wherein the element isolating region, (Figure 17 #73), is formed of an oxide film, (STI formation Col. 13 Lines 58-64), obtained by oxidizing the semiconductor substrate, (Figure 17 #60).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-12 & 20-25 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,670,234 Hsu et al.

10. Referring to claim 1, a semiconductor device comprising: a semiconductor substrate, (Figure 17 #400); flat-plate-shaped cavity, (Figure 17 #200 which the cavity is filled with n-type dopant), made in the semiconductor substrate, (Figure 17 #400); and an element isolating region, (Figure 17 #100), formed in the surface of the semiconductor substrate, (Figure 17 #400), and located at the sides the cavity, (Figure 17 #200).

11. Referring to claim 2, a semiconductor device, wherein the area of **the top** of the cavity, (Figure 17 #400), is larger than the area of **the base**, (Figure 17 #300), an element region provided at **the top** the cavity, (Figure 17 #200).

12. Referring to claim 3, a semiconductor device, wherein the element isolating region, (Figure 17 #100), and the cavity, (Figure 17 #200,) enclose the element region, (Figure 17 #100), provided at the top of the cavity, (Figure 17 #200), and electrically separate the element region, (Figure 17 #300), from the semiconductor substrate, (Figure 17 #400).

13. Referring to claim 4, a semiconductor device, wherein only one element region, (Figure 17 #300), provided at the top of the cavity, (Figure 17 #200).

14. Referring to claim 5, a semiconductor device, wherein **the base**, (Figure 17 #300), of the element isolating region is less deep than **the bottom** of the cavity, (Figure 17 #200), and deeper than **the top** of the cavity, (Figure 17 #200).

15. Referring to claim 6, a semiconductor device, wherein the element isolating region, (Figure 17 #100), is formed of an oxide film, (Col. 7 Lines 63-67), obtained by oxidizing the semiconductor substrate, (Figure 17 #400).

16. Referring to claim 7, a semiconductor device comprising: a semiconductor substrate; a plurality of flat-plate-shaped cavities, (Figure 17 #200 which the cavity is filled with n-type dopant), made in the semiconductor substrate, (Figure 17 #400); and an element isolating region, (Figure 17 #100), formed in the surface of the semiconductor substrate, (Figure 17 #400), between adjacent ones of the cavities, (Figure 17 #200), a part of the element isolating region, (Figure 17 #100), being exposed to the sides of the cavities, (Figure 17 #200).

17. Referring to claim 8, a semiconductor device, wherein the area of **the top** of each cavity, (Figure 17 #200), is larger than the area of **the base** of an element region, (Figure 17 #300), provided at **the top** of each the cavities, (Figure 17 #200), respectively.

18. Referring to claim 9, a semiconductor device, wherein the element isolating region, (Figure 17 #100), and the cavities, (Figure 17 #200), enclose the element regions, (Figure 17 #300), provided at the top of the cavities, (Figure 17 #200), and electrically separate the element regions, (Figure 17 #300), from the semiconductor substrate, (Figure 17 #400).

19. Referring to claim 10, a semiconductor device, wherein only one element region, (Figure 17 #300), is provided at the top of the cavity, (Figure 17 #200).

20. Referring to claim 11, a semiconductor device, wherein **the base**, (Figure 17 #300), of the element isolating region is less deep than **the bottom** of the cavities, (Figure 17 #200), and deeper than **the top** of the cavities, (Figure 17 #200).

21. Referring to claim 12, a semiconductor device, wherein the element isolating region, (Figure 17 #100), is formed of an oxide film, (Col. 7 Lines 63-67), obtained by oxidizing the semiconductor substrate, (Figure 17 #400).

22. Referring to claim 20, a method of fabricating a semiconductor device, comprising: making flat-plate-shaped cavities partly a semiconductor substrate, (Figure 17 #400); forming an insulating film, (Figure 17 #100), in the surface of the semiconductor substrate, (Figure 17 #400), between adjacent ones of the cavities, (Figure 17 #200), in such a manner that a part of the insulating film, (Figure 17 #100), is exposed the sides of the cavities, (Figure 17 #200), so as to electrically separate element regions, (Figure 17 #300), provided at the top of the adjacent cavities, (Figure 17 #200), from each other; and forming semiconductor elements, (Figure 17 #500), on the element regions, (Figure 17 #300).

23. Referring to claim 21, a method of fabricating a semiconductor device, wherein the insulating film, (Figure 17 #100), is formed by oxidizing, (Col. 7 Lines 63-67), the surface of the semiconductor substrate.

24. Referring to claim 22, a method of fabricating a semiconductor device, wherein the area of **the top** of each cavity, (Figure 17 #200), is larger than the area of **the base**, (Figure 17 #300), of the element region provided at **the top** of each of the cavities, (Figure 17 #200), respectively.

25. Referring to claim 23, a method of fabricating a semiconductor device, wherein the insulating film, (Figure 17 #100), and the cavities, (Figure 17 #200), enclose the element regions, (Figure 17 #300), and electrically separate the element regions, (Figure 17 #300), from the semiconductor substrate, (Figure 17 #400).

26. Referring to claim 24, a method of fabricating a semiconductor device, wherein only one element region, (Figure 17 #300), provided at the top of each of the cavities, (Figure 17 #200).

27. Referring to claim 25, a method of fabricating a semiconductor device, wherein **the base**, (Figure 17 #300), of the insulating film, (Figure 17 #100), is less deep than **the bottom** of the cavities, (Figure 17 #200), and deeper than **the top** of the cavities, (Figure 17 #200).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Victor A Mandala Jr. whose telephone number is (571) 272-1918. The examiner can normally be reached on Monday through Thursday from 8am till 6pm..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on (571) 272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

VAMJ
11/04/04